EECS 2077 Test #3, Winter 2014 Name:_____

#1 ____/25 pts **Allowed materials: 3 pages of 1-sided equation sheets, writing utensil, calculator.**
#2 ____/25 pts **Remember – we use cgs units! Centimeter/gram/second.**
#3 ____/20 pts kT = 0.026 eV (300K) ε_0=8.854x10^{-14} F/cm ε_r(Si)=11.8 / ε_r(SiO_2)=4.0
#4 ____/30 pts q= 1.6x10^{-19} C n_i(Si)=1.5x10^{10} / cm^3

Optional Feedback
Rate the length of this test: ***short*** ☐ ***long*** ☐ ***OK*** ☐
Rate the difficulty of this test: ***easy*** ☐ ***hard*** ☐ ***OK*** ☐

1.) Multiple choice questions, for MOSFETs. Only one answer for each. [5 pts each]

a) Below threshold voltage and with a source-to-drain voltage applied, the MOSFET will not allow significant current flow from source to drain because:

[ ] – the channel is experiencing inversion
[ ] – the channel under the gate is depleted of carriers
[ ] - at least one PN junction is reversed biased
[ ] - of Voodoo magic.

b) Below threshold, if I double the charge on the gate electrode, the charge on the other side of the oxide will:
[ ] – also double
[ ] – increase by square root of 2
[ ] - increase by e^2
[ ] - explode with excitement.

c) For the case of applying DC bias to switch a transistor, the impedance at the gate of a MOSFET is:
[ ] – zero
[ ] – infinite
[ ] - same as the base of BJT
[ ] – suffering from severe ennui.

d) The minimum capacitance seen by the gate electrode occurs at:
[ ] - half of the threshold votlage
[ ] - well above threshold voltage
[ ] - right below threshold votlage
[ ] - 2 AM on Friday nights on the way home.

e) Which of these mechanisms of charge transport makes Flash memory different from other MOSFETs:
[ ] - drift
[ ] - diffusion
[ ] - tunneling
[ ] - teleportation.

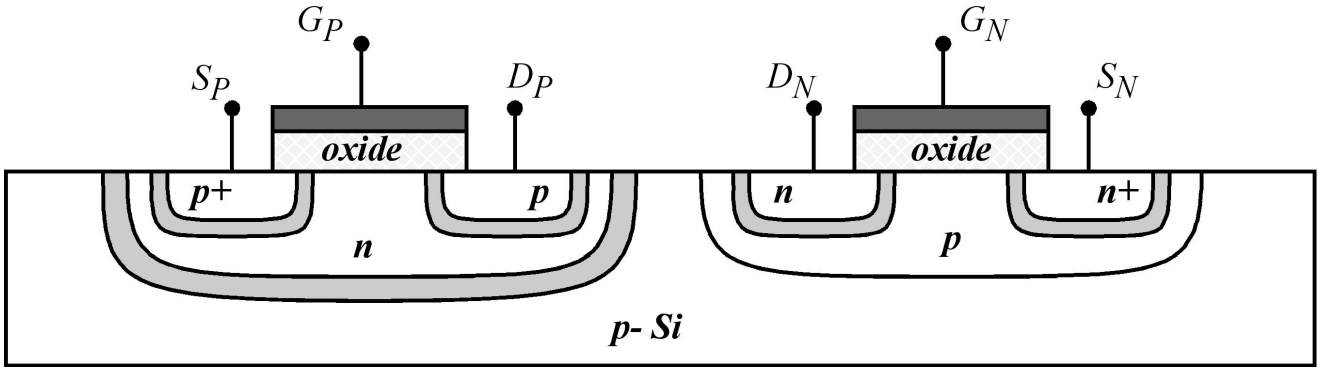
EECS 2077 Test #3, Winter 2014 Name:_____

2) 25 pts. The following is for an ideal pair of NMOS and PMOS devices that form the basis for a logic inverter with a threshold voltage of 3V. Perform the following. QUALITATIVE / NO CALCULATIONS NEEDED!

(a) [10 pts.]

FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw a ground on the NMOS source and +5V on the PMOS source.

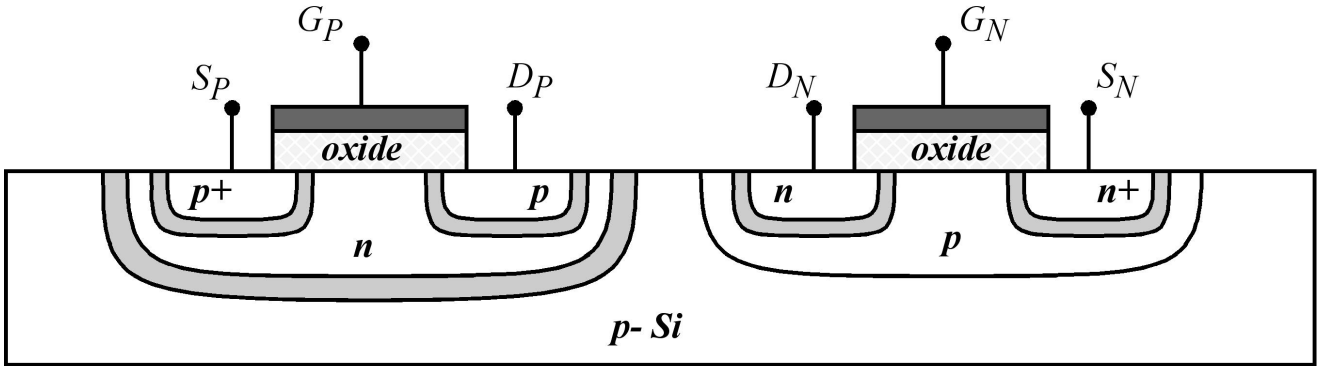
SECOND: using lines with arrows, or directly on the diagram, label as many voltages as possible on each semiconductor region (there are 7 different regions below) **for the case of 0V applied to V_{IN}**, and also label the voltage at V_{OUT} (just label the voltages as 0V, or 5V, and don't worry about labeling the voltages close to the gate oxide).



(b) [15 pts.]

FIRST: draw an input voltage (V_{IN}) that connects to both gates (G), draw an output voltage (V_{OUT}) that connects to both drains (D), draw -10 V on the NMOS source and -5V on the PMOS source.

SECOND: label the diagram similar to how you did for part (a), but do it for the case where the output voltage is -5 V. Note, now you have to label the input voltage too! You may only label it with voltages such as -15V, -10V, -5 V, 0V, 5V, 10V, 15V. Do not use any more voltage than is needed to exceed Vth.



3.) [20 pts.] Lets play the drift versus diffusion game! Circle the correct answer for each:

a) Dominates the input current required at the gate of a JFET: [5 pts.]

DRIFT DIFFUSION BOTH NEITHER

b) Dominates the input current required at the gate of a MESFET. [5 pts.]

DRIFT DIFFUSION BOTH NEITHER

c) Is the main reason why you need input current at the base of a well-designed BJT. [5 pts.]

DRIFT DIFFUSION BOTH NEITHER

d) Dominates the flow of carriers from drain to source in a MOSFET that is above threshold. [5 pts.]

DRIFT DIFFUSION BOTH NEITHER

4) [30 pts] Question related to an p-MOS transistor with the following parameters:

The gate electrode 'metal' is n+ poly Silicon.

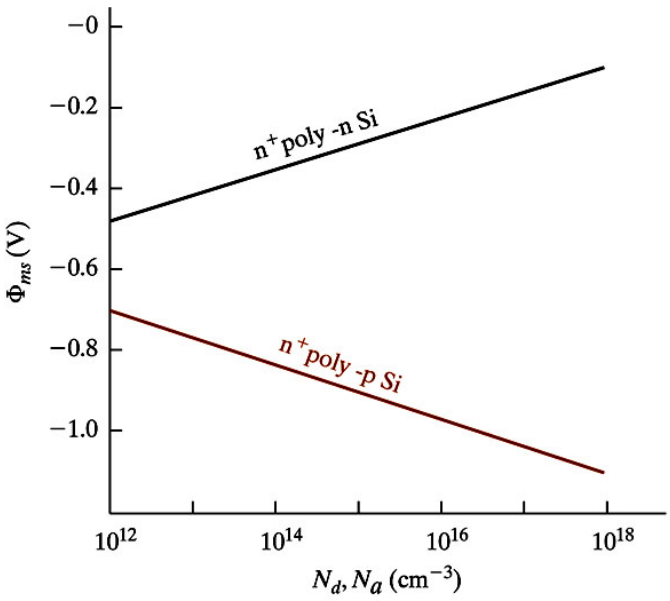
The substrate is doped with Phosphorus to the level of Nd=10^{17}/cm^3.

In the plot shown at right, the curves are labeled as 'gate material – substrate material'.

The gate oxide is has a thickness of 10 nm and a dielectric constant of 4.

There is an interface charge (Qi) of -70 nC/cm^2.

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{D,\max}}{C_i} + 2\phi_f$$



a) provide the value for how much the Fermi level in the substrate has been shifted from the intrinsic Fermi level due to doping (deeper into the substrate, where the bands are flat) [5 pts]:

b) calculate the capacitance per unit area of the gate oxide [5 pts]:

c) provide the value for the maximum depletion charge [5 pts]

d) provide the value for how much threshold voltage is influenced by the fact that the Fermi level of the gate electrode and the Fermi level of the substrate Si, have to shift to match up [5 pts]:

e) calculate the threshold votlage for this device [10 pts]:

EXTRA SPACE